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UTILITY PATENT APPLICATION TRANSMITTAL
(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.	:	40176/DBP/Y35
Inventor(s)	:	Yang-Woon Na, and Jong-Hun You
Title	:	FLAT PANEL DISPLAY AND METHOD OF FABRICATING SAME
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Box Patent Application
Washington, D.C. 20231

Date: August 23, 2000

1. X **FEE TRANSMITTAL FORM** *(Submit an original, and a duplicate for fee processing).*

2. **IF A CONTINUING APPLICATION**
   ___ This application is a of patent application No. .

   Prior application information: Examiner ; Group Art Unit:

   ___ This application claims priority pursuant to 35 U.S.C. §119(e) and 37 CFR §1.78(a)(4), to provisional Application No. .

3. **APPLICATION COMPRISED OF**

   Specification
   23 Specification, claims and Abstract (total pages)

   Drawings
   16 Sheets of drawing(s) (FIGS. 1 to 23)

   Declaration and Power of Attorney
   X Newly executed
   ___ Unexecuted declaration
   ___ Copy from a prior application (37 CFR 1.63(d))(for continuation and divisional)

4. ___ **Microfiche Computer Program** *(Appendix)*

5. ___ **Nucleotide and/or Amino Acid Sequence Submission** *(if applicable, all necessary)*
   ___ Computer Readable Copy
   ___ Paper Copy (identical to computer copy)
   ___ Statement verifying identity of above copies

6. **ALSO ENCLOSED ARE**
   ___ Preliminary Amendment
   ___ A Petition for Extension of Time for the parent application and the required fee are enclosed as separate papers
   ___ Small Entity Statement(s)
   ___ Statement filed in parent application, status still proper and desired
   ___ Copy of Statement filed in provisional application, status still proper and desired

UTILITY PATENT APPLICATION TRANSMITTAL
(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.: 40176/DBP/Y35

X An Assignment of the invention with the Recordation Cover Sheet and the recordation fee are enclosed as separate papers
___ This application is owned by pursuant to an Assignment recorded at Reel , Frame
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___ Other

7. **CORRESPONDENCE ADDRESS**

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Respectfully submitted,

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DBP/aam

FLAT PANEL DISPLAY AND METHOD OF FABRICATING SAME

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to a flat panel display and a method of fabricating the same and, more particularly, to a flat panel display which has gate electrodes for making electrons to be emitted from electron emission sources, and a focusing electrode for controlling flow of the emitted electrons.

(b) Description of the Related Art

Generally, a flat panel display (FPD) has a faceplate, a backplate, and a side wall that are combined together to form a vacuum tight cell. The vacuum degree of the cell is established to be about 10^{-7} torr.

In case such a flat panel display, it is difficult to constantly maintain the cell gap due to the difference between the internal pressure and the external atmospheric pressure. For this reason, one or more spacers are provided within the cell to maintain the cell gap in a constant manner.

In the case of high voltage flat panel displays, the distance between the faceplate and the backplate reaches 1 ㎜ or more. In this case, the electrons emitted from the electron sources do not land on the correct phosphors but strike the neighboring incorrect phosphors. In order to prevent such a mis-landing, the conventional high voltage flat panel display is provided with a focusing electrode for controlling flow of the emitted electrons.

In consideration of the above problems, U. S. Patent No. 5,650,690

discloses a field emission display that has a gripper disposed on the faceplate, a locator disposed on the backplate, and a spacer wall interposed between the gripper and the locator to secure the internal space of the device in an effective manner. A focusing electrode surrounds emitters to control flow of the electrons emitted from the emitters.

In the above structure, the locator and the focusing electrode are formed through depositing a photoresist film onto a substrate based on spin coating or screen printing, and performing photolithography with respect to the photoresist film. In such a photolithography process, since thermal expansion coefficients of the electrode formation material and the plate formation material are different, their physical properties are liable to be deteriorated, and, after vacuum deposition, their moisture contents are slowly flown out while making damage to the minute emitters, decreasing the device life span. Furthermore, a high cost paste is deposited onto the plate by several tens micrometers to form electrodes, resulting in increased production cost.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a flat panel display which can be fabricated in a stable manner at an economic cost.

This and other objects may be achieved by a flat panel display including a faceplate, a backplate combined with the faceplate to form a vacuum tight cell, and a light emission unit placed within the cell to emit light from the cell. The backplate has a plurality of electron emission sources. A

frame is mounted on the backplate with opening portions. The electron emission sources are exposed through the opening portions of the frame toward the faceplate. A plurality of spacers are formed on the frame such that the spacers are positioned at a non-display area within the cell. A plurality of gate electrodes are formed at a surface of the frame with a predetermined pattern. The gate electrodes has opening portions communicating with the opening portions of the frame.

According to one aspect of the present invention, a method of fabricating a flat panel display includes the steps of forming a plurality of cathode electrodes on a first substrate, and forming emitters on the cathode electrodes as electron emission sources. A frame is then mounted onto the first substrate. The frame has opening portions corresponding to the emitters, a plurality of spacers positioned at a non-display area to maintain a cell gap, and a plurality of gate electrodes formed on a surface thereof. An anode electrode is formed on a second substrate. A plurality of phosphor layers are formed on the anode electrode. Finally, the first substrate is combined with the second substrate to thereby form a vacuum tight cell.

According to another aspect of the present invention, a method of fabricating a flat panel display includes the steps of forming a plurality of cathode electrodes on a first substrate, and forming emitters on the cathode electrodes as electron emission sources. A frame is then mounted onto the first substrate. The frame has opening portions corresponding to the emitters, a plurality of spacers positioned at a non-display area to maintain a cell gap, a

plurality of gate electrodes formed on a surface thereof, and a focusing electrode formed on an opposite surface thereof. A plurality of anode electrodes are formed on a second substrate. A plurality of phosphors are formed on the anode electrodes. Finally, the first substrate is combined with the second substrate to thereby form a vacuum tight cell.

According to still another aspect of the present invention, in a method of fabricating a flat panel display, a plurality of cathode electrodes are formed on a first substrate with a predetermined pattern. Thereafter, a photosensitive dielectric layer is formed on the first substrate through screen-printing a photosensitive dielectric paste onto the entire surface of the first substrate, and drying the paste. The portions of the photosensitive dielectric layer corresponding to a pixel area are removed through partially exposing the photosensitive dielectric layer to light, and developing the light-exposed dielectric layer. Electron emission sources are formed at the removed portions of the dielectric layer. A plurality of opening portions are formed at a frame. The frame is formed with a photosensitive glass. A plurality of gate electrodes are formed on a surface of the frame. A plurality of spacers are formed on the frame at a non-display area. An anode electrode is formed on a second substrate. A plurality of phosphor layers are formed on the anode electrode. Finally, the frame is mounted onto the first substrate such that the electron emission sources are placed within the opening portions of the frame, and the second substrate is combined with the first substrate to thereby form a vacuum tight cell.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

Fig. 1 is a cross sectional view of a flat panel display with a frame according to a first preferred embodiment of the present invention;

Fig. 2 is a perspective view of a frame for the flat panel display shown in Fig. 1;

Fig. 3 is a perspective view of spacers for the flat panel display shown in Fig. 1;

Figs. 4 to 9 are schematic views illustrating the steps of processing a frame for the flat panel display shown in Fig. 1;

Fig. 10 is a perspective view of gate electrodes arranged on a frame for the flat panel display shown in Fig. 1;

Fig. 11 is a perspective view of a frame mounted on a backplate for the flat panel display shown in Fig. 1;

Fig. 12 is a cross sectional view of a flat panel display according to a second preferred embodiment of the present invention;

Fig. 13 is a cross sectional view of a flat panel display according to a third preferred embodiment of the present invention;

Fig. 14 is a perspective view of the flat panel display shown in Fig. 13;

Fig. 15 is a perspective view of gate electrodes arranged on a frame for the flat panel display shown in Fig. 13;

Fig. 16 is a perspective view of a focusing electrode formed on a frame for the flat panel display shown in Fig. 13;

Fig. 17 is an exploded perspective view of a flat panel display according to a fourth preferred embodiment of the present invention;

Fig. 18 is a combinatorial sectional view of the flat panel display shown in Fig. 17;

Figs. 19 to 21 illustrate the steps of forming a dielectric layer for the flat panel display shown in Fig. 17; and

Figs. 22 and 23 illustrate the steps of forming electron emission sources for the flat panel display shown in Fig. 17.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

Fig. 1 is a cross sectional view of a flat panel display according to a first preferred embodiment of the present invention where a field emission display (FED) is exemplified as the flat panel display.

As shown in Fig. 1, the field emission display includes a faceplate 1, and a backplate 3 spaced apart from the faceplate 1 with a predetermined distance while proceeding parallel thereto. The faceplate 1 is combined with the backplate 3 to thereby form a vacuum tight cell 5. In the formation of the

cell 5, a side glass 7 is interposed between the faceplate 1 and the backplate 3.

The faceplate 1 is sequentially overlaid with anode electrodes 9 with a predetermined pattern (ex. stripe), and a plurality of R, G and B phosphors 11. The phosphors 11 are formed on the anode electrodes 9 through slurry coating or screen printing. A black matrix 13 surrounds the phosphors 11.

In contrast, the backplate 3 is sequentially overlaid with cathode electrodes 17 with a predetermined pattern (ex. stripe), and a plurality of face emitters 15 that function as the electron source for striking the phosphors 11. It is preferable that the emitters 15 are formed with carbon nano-tubes.

A frame 21 is mounted at the backplate 3, and gate electrodes 19 are formed on the frame 21 to make electrons to be extracted from the emitters 15.

As shown in Fig. 2, the frame 21 has a size corresponding that of the backplate 3, and internally has a plurality of opening portions 21a. The opening portions 21a of the frame 21 are formed such that they correspond to the pixels of the phosphors 9 and the emitters 15. The frame 21 further has spacers 23 for maintaining the cell gap in a constant manner.

The spacers 23 are formed at the non-display area integral to the frame 21. The spacers 23 may be formed with a shape of a cylinder, a polyhedron with a section of rectangle or cross, or a thin sheet.

Furthermore, a support 25 placed at the same plane as the spacers 23 is integrally formed at a side portion of the frame 21 to maintain the cell gap together with the spacers 23.

In the meantime, the frame 21 is formed with a photosensitive glass

through suffering separate processing steps. Figs. 4 to 9 illustrate the steps of processing the frame 21 while focusing at one of the opening portions 21a formed at the frame 21 for convenience in illustration.

As shown in the drawing, a photosensitive glass 27 with a predetermined thickness is exposed to light through masks 29 and 31 for about 30 minutes. The masks 29 and 31 has opening portions 29a and 31a, respectively. Then, the light-exposed glass 27 is moved into a furnace (not shown), and suffers two stepped heat-treatments at 500℃ for one hour, and at 600℃ for one hour. Thereafter, an over-etching prevention layer 33 is formed on an one-sided surface of the glass 27 as a photoresist. The over-etching prevention layer 33 is to prevent the surface of the glass 27 from being over-etched in the subsequent etching step.

In the etching step, the glass 27 is dipped into an etching solution of HF 10% for 10-40 minutes. As a result, heat-treated portions are removed from the glass 27, and the glass 27 has a shape shown in Fig. 8. Finally, as shown in Fig. 9, the over-etching prevention layer 33 is removed from the glass 27 to complete a frame 21 with spacers 23.

As shown in Fig. 10, the gate electrodes 19 are formed on the frame 21 with a predetermined thickness and a stripe pattern. The gate electrodes 19 have opening portions 19a corresponding to the opening portions 21 of the frame 21. The gate electrodes 19 are preferably formed through vapor deposition based on aluminum (Al) or indium tin oxide (ITO).

Fig. 11 is a perspective view of the frame 21 mounted on the backplate

3. As shown in Fig. 11, the frame 21 is mounted onto the backplate 3 such that the emitters 15 are arranged within the opening portions 21a thereof. Of course, the spacers 23 are naturally placed at the non-display region within the cell 5. That is, the position control of the plurality of spacers 23 can be performed simultaneously with the mount of the frame 21 onto the backplate 3.

Fig. 12 is a cross sectional view of a field emission display according to a second preferred embodiment of the present invention. In this preferred embodiment, other components and structures of the field emission display are the same as those related to the first preferred embodiment except that the spacer fixation structure formed at the frame is differentiated. That is, in the previous preferred embodiment, the spacers are integrally formed at the frame, whereas, in this preferred embodiment, the spacers 23 are not formed with the frame 21 in a body, but fixed to the frame 21 by way of fixation holders 21b.

The spacer fixation holders 21b are breakthrough holes formed at the frame 21. The spacers 23 are made separately from the frame 21, and one-sided end portions of the spacers 23 are fitted within the holders 21b. Of course, as described above, the spacers 23 may be formed with various shapes such as a cylinder. The holder 21b may have a shape corresponding to the shape of the spacer 23. For example, when the spacer is shaped with a cylinder, the holder 21b may be formed with a circular opening portion. When the spacer 23 is shaped with a section of rectangle, the holder 21b may be formed with a rectangular opening portion.

As the spacers 23 are not formed with the frame 21 in a body, in the

formation process of the frame 21, a mask for exposing the photosensitive glass to light is provided only at one-sided surface of the photosensitive glass, and the over-etching prevention layer is not required. Of course, other processing steps for forming the frame 21 are performed in the same way as that related to the first preferred embodiment.

Like the above, in the structure of the field emission display according to the second preferred embodiment, separate spacers 23 are fixed to the frame 21, and the frame 21 with the spacers 23 is mounted onto the backplate 3. In this way, the processing steps can be simplified while accompanying with other advantageous effects.

Fig. 13 is a cross sectional view of a field emission display according to a third preferred embodiment of the present invention. In this preferred embodiment, a photosensitive glass-based frame 21 is also provided between the faceplate 1 and the backplate 3. In addition to the gate electrodes 19, a focusing electrode 33 is formed on the frame 21 to control flow of electrons extracted from emitters 15.

Specifically, the frame 21 has a size corresponding to that of the backplate 3, and is internally formed with a plurality of opening portions 21a, and spacers 23 for maintaining the cell gap in a constant manner.

As shown in Fig. 14, the spacers 23 are integrally formed at both upper and lower surfaces of the frame 21 such that they are positioned at the non-display area within the cell. As previously described, the spacers 23 may be shaped with a cylinder, a polyhedron having a section of rectangle or cross, or

a thin sheet.

As the spacers 23 are formed at both upper and lower surfaces of the frame 21, the formation process thereof does not include the step of forming an over-etching prevention layer while other processing steps being the same as those related to the first preferred embodiment.

As shown in Fig. 15, the gate electrodes 19 are formed on the one-sided surface of the frame 21 (facing the backplate 3) with a stripe pattern, and, as shown in Fig. 16, the focusing electrode 33 is entirely formed on the opposite surface of the frame 21 (facing the anode electrode 9) with a predetermined thickness. Of course, the gate electrodes 19, and the focusing electrode 33 are provided with opening portions 19a and 33a corresponding to the opening portions 21a of the frame 21.

The gate electrodes 19 and the focusing electrode 33 are preferably formed through vapor deposition based on aluminum or indium tin oxide. In this preferred embodiment, the gate and focusing electrodes 19 and 33 are formed with different materials.

Fig. 17 is an exploded perspective view of a field emission display according to a fourth preferred embodiment, and Fig. 18 is a combinatorial sectional view of the field emission display shown in Fig. 17.

As shown in the drawings, the field emission display includes a faceplate 42 and a backplate 44 that are combined with each other via a frit 40.

A plurality of cathode electrodes 46 are formed on the backplate 44 with a stripe pattern, and carbon nano-tubes 48 are separately formed on the

cathode electrodes 46 as filed emitters while being spaced apart from each other with a predetermined distance.

Furthermore, a dielectric layer 50 based on a photosensitive material is formed on the backplate 44 except the portions where the carbon nano-tubes 48 are placed.

In contrast, an anode electrode 52 is formed on the faceplate 42 with a predetermined pattern, and a plurality of phosphors 54 are formed on the anode electrode 52.

A frame 56 based on a photosensitive glass is provided between the plates 42 and 44, and the plates 42 and 44 are combined with each other via a frit 40. The frame 56 has opening portions 56a corresponding to the carbon nano-tubes 48, and gate electrodes 58 are formed on the one-sided surface of the frame 56 (facing the faceplate 42) to make electrons to be extracted from the carbon nano-tubes 48.

The gate electrodes 58 have opening portions 58a communicating with the opening portions 56a of the frame 56. The gate electrodes 58 proceed perpendicular to the cathode electrodes 46.

Furthermore, in order to maintain the cell gap in a constant manner, a plurality of spacers 60 are arranged at the non-display area while being interposed between the plates 42 and 44.

In this preferred embodiment, the process of fabricating the field emission display are performed in the following way.

Roughly, relevant components are first formed at the backplate 44 and

the faceplate 42, respectively. Then, the gate electrodes 58 are formed at the frame 56. Finally, the faceplate 42, the backplate 44, and the frame 56 are combined together.

Specifically, as shown in Fig. 19, silver paste is screen-printed onto the backplate 44 in a stripe pattern, and heat-treated to thereby form cathode electrodes 46. Positive photosensitive dielectric paste is screen-printed onto the cathode electrodes 46, and dried to thereby form a dielectric layer 50.

Thereafter, as shown in Fig. 20, a mask 62 with a plurality of light exposing holes 62a corresponding to the pixel area is mounted over the dielectric layer 50, and the dielectric layer 50 is exposed to light for a predetermined time so that the light exposed portions thereof bear increased solubility. Then, as shown in Fig. 21, the dielectric layer 50 is developed, and the light exposed portions thereof bearing increased solubility are removed from the dielectric layer 50 to thereby form opening patterns.

The opening patterns of the dielectric layer 50 are to receive carbon nano-tubes 48.

In order to form such carbon nano-tubes 48, as shown in Fig. 22, a carbon nano-tube paste 48' is first screen-printed at the opening patterns of the dielectric layer 50. Thereafter, the backplate 44 is baked at 450-500 under the atmospheric pressure such that the binder content is evaporated from the paste 48'.

As shown in Fig. 23, the carbon nano-tubes 48 are surface-treated through grinding to obtain uniform surfaces.

Meanwhile, the frame 56 is formed with a photosensitive glass, and passes through the steps of light exposing, heat-treating, and etching to form a plurality of opening portions 56a. The gate electrodes 58 are formed through screen-printing metallic silver paste onto a surface of the frame 56 with a stripe pattern, and drying and baking the paste.

After the gate electrodes 58 are formed on the frame 56, a plurality of spacers 60 are formed on the frame 56 at the non-display area.

By contrast, the formation process of the anode electrode 52 and the phosphors 54 at the faceplate 42 is made in the conventional way.

Finally, the frame 56 is mounted onto the backplate 44 such that the carbon nano-tubes 48 are exposed through the opening portions 56a thereof, and fixed to the backplate 44. Then, the faceplate 42 is mounted onto the frame 56, and fixed to the frame 56 to thereby complete a field emission display.

As described above, in the inventive flat panel display, the gate electrodes, the focusing electrode and the spacers are formed at the backplate not in a direct manner but via a separate frame, the problems of damage to the products and high production cost involved in the prior art-based flat panel displays can be effectively solved.

Furthermore, the above-described structure related to the field emission display may be applied to other flat panel displays such as flat CRTs.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing

from the spirit and scope of the present invention as set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A flat panel display comprising:

a faceplate;

a backplate combined with the faceplate to form a vacuum tight cell, the backplate having a plurality of electron emission sources;

a light emission unit placed within the cell to emit light from the cell;

a frame mounted on the backplate, the frame having opening portions, the electron emission sources being exposed through the opening portions toward the faceplate;

a plurality of spacers formed on the frame such that the spacers are positioned at a non-display area within the cell; and

a plurality of gate electrodes formed at a surface of the frame with a predetermined pattern, the gate electrodes having opening portions communicating with the opening portions of the frame.

2. The flat panel display of claim 1 wherein the frame is formed with a photosensitive glass.

3. The flat panel display of claim 1 further comprising a focusing electrode formed on an opposite surface of the frame with a predetermined pattern, the focusing electrode having opening portions communicating with the opening portions of the frame.

4. The flat panel display of claim 1 wherein the light emission unit comprises:

a plurality of cathode electrodes formed on the backplate within the cell;

emitters formed on the cathode electrodes as the electron emission sources while being placed within the opening portions of the frame;

anode electrodes formed on the faceplate within the cell with a predetermined pattern,; and

a plurality of phosphors formed on the anode electrode.

5. The flat panel display of claim 4 wherein the emitters are face-emitters.

6. The flat panel display of claim 5 wherein the emitters are formed with carbon nano-tubes.

7. The flat panel display of claim 1 wherein the spacers are formed on a one-sided surface of the frame.

8. The flat panel display of claim 1 wherein the spacers are formed on both surfaces of the frame opposite to each other.

9. The flat panel display of claim 1 wherein the spacers and the frame are formed in a body with the same material.

10. The flat panel display of claim 7 wherein the frame has holders, and the spacers are fitted within the holders.

11. The flat panel display of claim 1 wherein a support is formed at a side portion of the frame in a body such that the support fixedly contacts the faceplate.

12. The flat panel display of claim 1 wherein a support is formed at a side portion of the frame in a body such that the support is fitted between the faceplate and the backplate.

13. The flat panel display of claim 4 further comprising a dielectric layer formed on the backplate except the portions where the emitters are placed.

14. The flat panel display of claim 13 wherein the dielectric layer is formed with a photosensitive material.

15. A method of fabricating a flat panel display, the method comprising the steps of:

forming a plurality of cathode electrodes on a first substrate;

forming emitters on the cathode electrodes as electron emission sources;

mounting a frame onto the first substrate, the frame comprising opening portions corresponding to the emitters, a plurality of spacers positioned at a non-display area to maintain a cell gap, and a plurality of gate electrodes formed on a surface thereof ;

forming an anode electrode on a second substrate;

forming a plurality of phosphor layers on the anode electrode; and

combining the first substrate with the second substrate to thereby form a vacuum tight cell.

16. A method of fabricating a flat panel display, the method comprising the steps of:

forming a plurality of cathode electrodes on a first substrate;

forming emitters on the cathode electrodes as electron emission sources;

mounting a frame onto the first substrate, the frame comprising opening portions corresponding to the emitters, a plurality of spacers positioned at a non-display area to maintain a cell gap, a plurality of gate electrodes formed on a surface thereof, and a focusing electrode formed on an opposite surface thereof;

forming an anode electrode on a second substrate;

forming a plurality of phosphor layers on the anode electrode; and

combining the first substrate with the second substrate to thereby form a vacuum tight cell.

17. The method of claim 15 wherein the frame is formed through the steps of:

mounting masks having predetermined opening patterns over both upper and lower surfaces of a photosensitive glass one by one;

exposing the photosensitive glass to light through the masks;

heat-treating the photosensitive glass;

depositing an over-etching prevention layer onto the photosensitive glass;

etching the photosensitive glass; and

removing the over-etching prevention layer from the photosensitive glass.

18. The method of claim 16 wherein the gate electrodes, and the focusing electrode are formed with aluminum or indium tin oxide through vapor deposition.

19. The method of claim 15 wherein the frame is formed through the steps of:

mounting a mask with a predetermined opening pattern onto a surface of a photosensitive glass;

exposing the photosensitive glass through the mask;

heat-treating the photosensitive glass; and

etching the photosensitive glass.

20. The method of claim 15 wherein the frame has spacer fixation holders at the non-display area, and the spacers are fitted within the spacer fixation holders.

21. The method of claim 16 wherein the frame is formed through the steps of:

mounting masks having predetermined opening patterns over both upper and lower surfaces of a photosensitive glass one by one;

exposing the photosensitive glass to light through the masks; and

heat-treating the photosensitive glass.

22. A method of fabricating a flat panel display, the method comprising the steps of:

forming a plurality of cathode electrodes on a first substrate with a predetermined pattern;

forming a photosensitive dielectric layer through screen-printing a photosensitive dielectric paste onto the entire surface of the first substrate, and drying the paste;

removing portions of the photosensitive dielectric layer corresponding to a pixel area through partially exposing the photosensitive dielectric layer to light, and developing the light-exposed dielectric layer;

forming electron emission sources at the removed portions of the dielectric layer;

forming a plurality of opening portions at a frame, the frame being formed with a photosensitive glass;

forming a plurality of gate electrodes on a surface of the frame;

forming a plurality of spacers on the frame at a non-display area;

forming an anode electrode on a second substrate;

forming a plurality of phosphor layers on the anode electrode; and

forming a vacuum tight cell through mounting the frame onto the first substrate such that the electron emission sources are placed within the opening portions of the frame, and combining the second substrate with the first substrate.

23. The method of claim 22 wherein the electron emission sources are formed through the steps of:

screen-printing a carbon nano-tube paste onto the cathode electrodes; and

heat-treating and surface-treating the printed carbon nano-tube paste.

24. The method of claim 22 wherein the opening portions of the frame are formed through the steps of:

mounting a mask with a predetermined opening pattern over a surface

of a photosensitive glass, and exposing the photosensitive glass to light through the mask;

heat-treating the photosensitive glass to light; and

etching the photosensitive glass such that the light exposed portions are removed from the photosensitive glass.

25. The method of claim 22 wherein the gate electrodes of the frame are formed through the steps of:

printing a metallic paste onto the frame with a predetermined pattern such that the opening portions of the frame are exposed to the outside; and

drying and baking the printed metallic paste.

ABSTRACT OF THE DISCLOSURE

A flat panel display includes a faceplate, a backplate combined with the faceplate to form a vacuum tight cell, and a light emission unit placed within the cell to emit light from the cell. The backplate has a plurality of electron emission sources. A frame is mounted on the backplate with opening portions. The electron emission sources are exposed through the opening portions of the frame toward the faceplate. A plurality of spacers are formed on the frame such that the spacers are positioned at a non-display area within the cell. A plurality of gate electrodes are formed at a surface of the frame with a predetermined pattern. The gate electrodes has opening portions communicating with the opening portions of the frame.

FIG.1

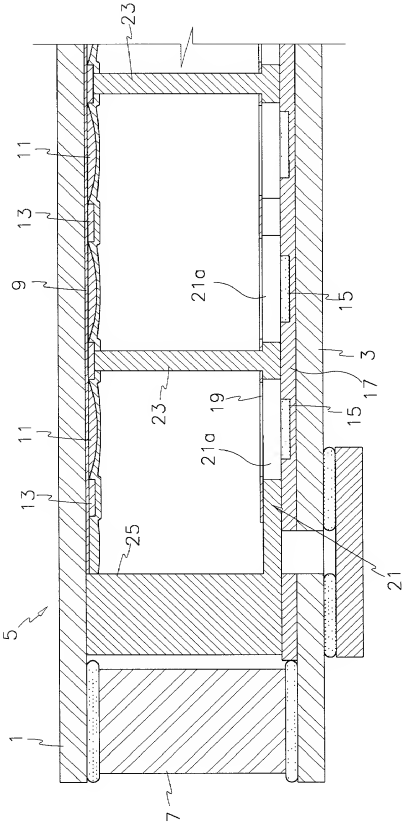


FIG.2

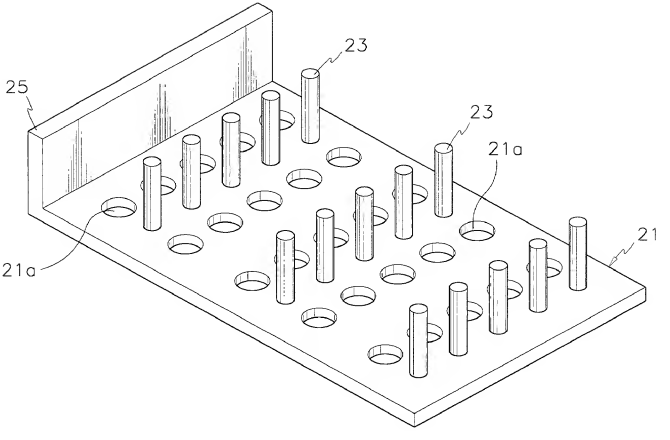


FIG.3

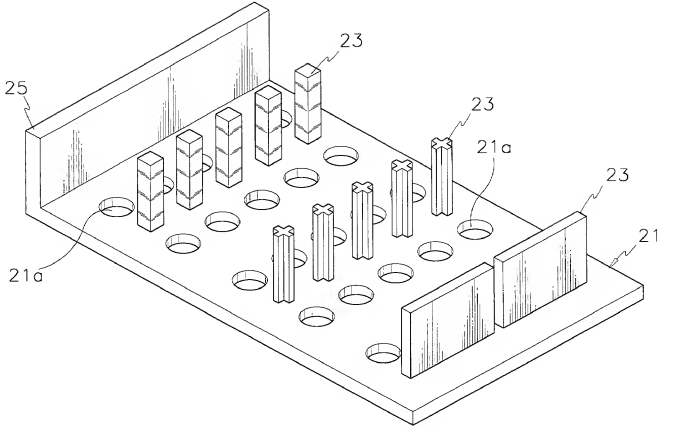


FIG.4

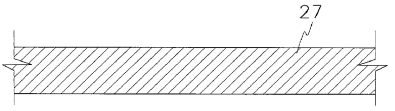


FIG.5

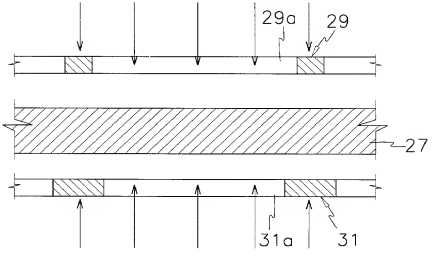


FIG.6

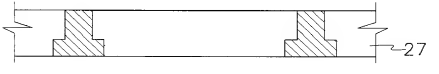


FIG.7

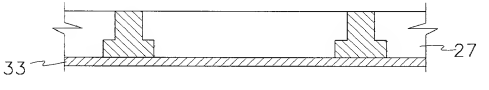


FIG.8

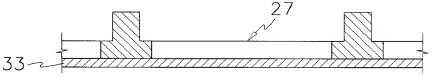


FIG.9

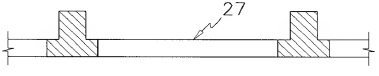


FIG.10

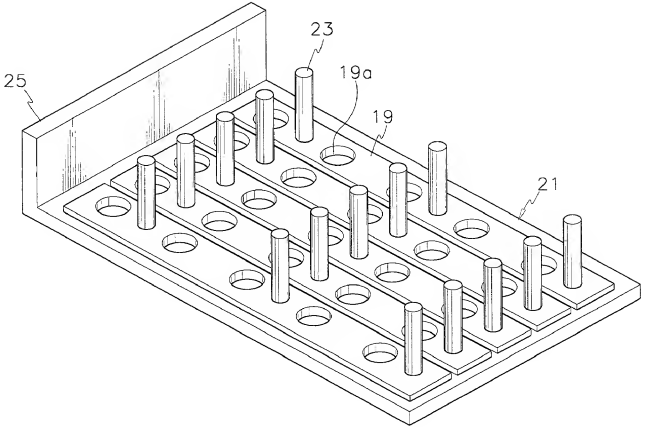


FIG.11

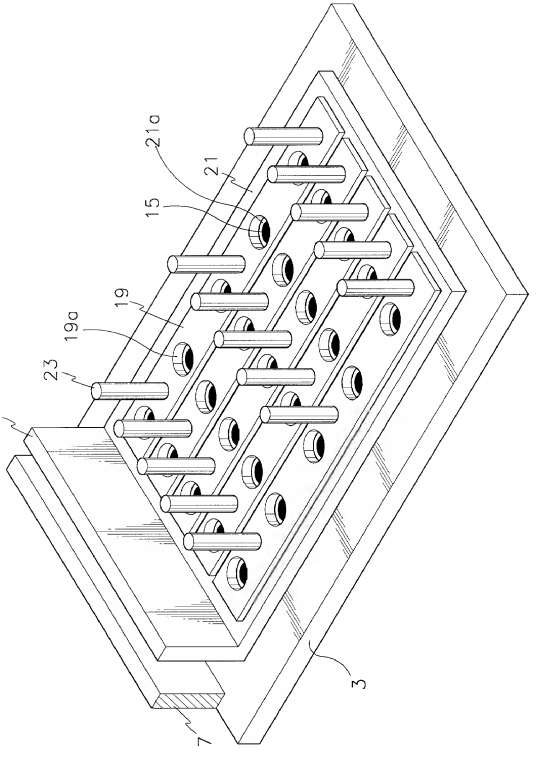


FIG.12

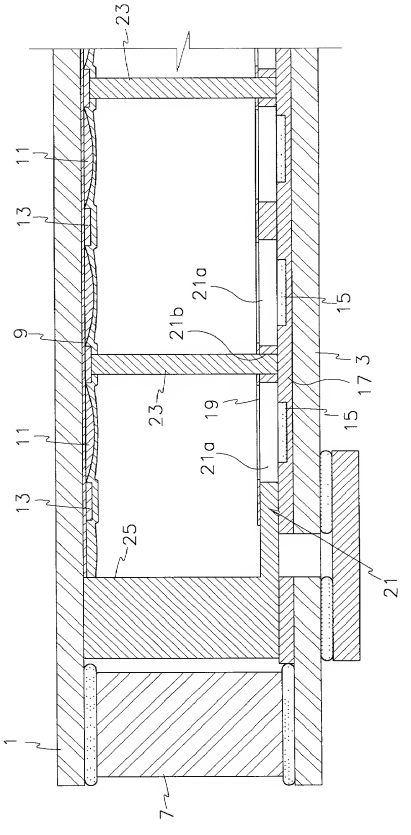


FIG. 13

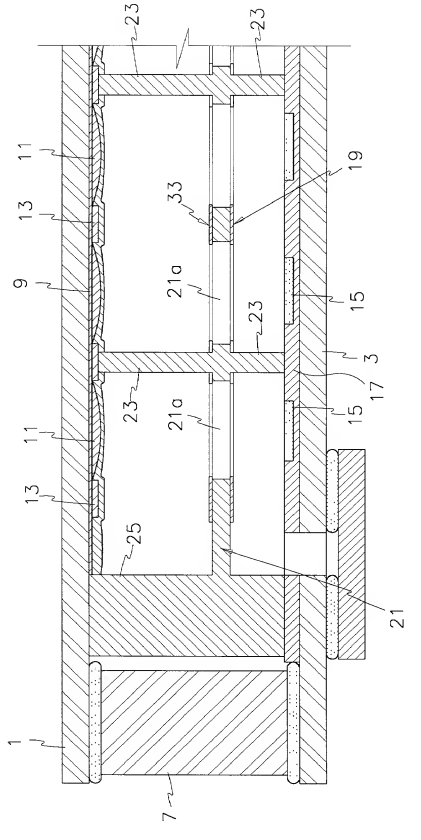


FIG.14

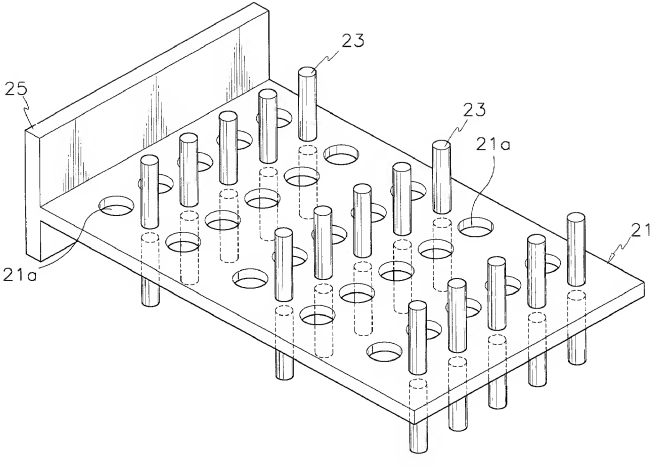


FIG.15

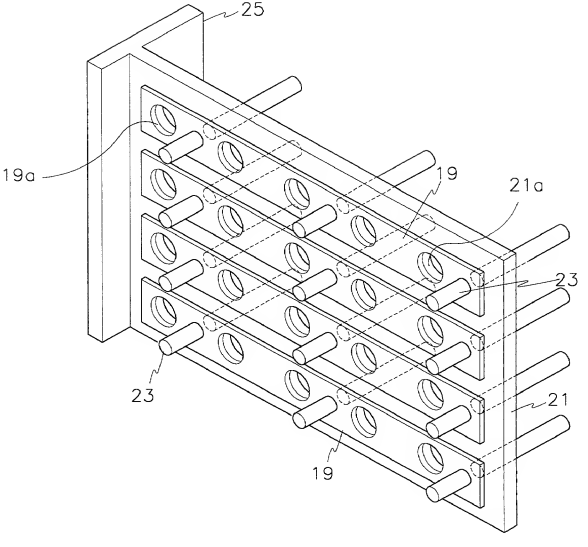


FIG.16

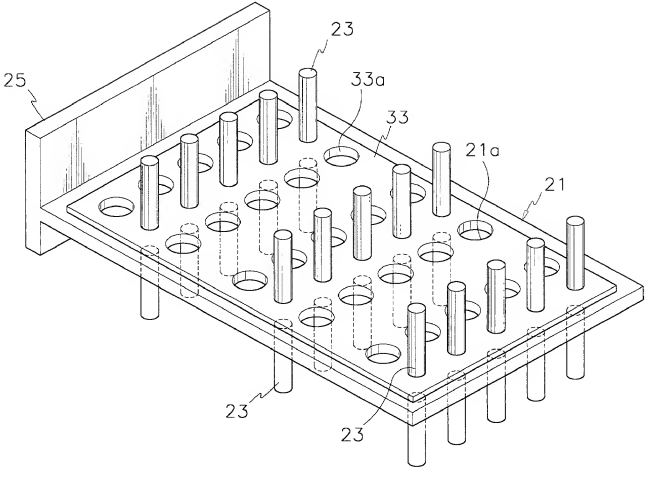


FIG. 17

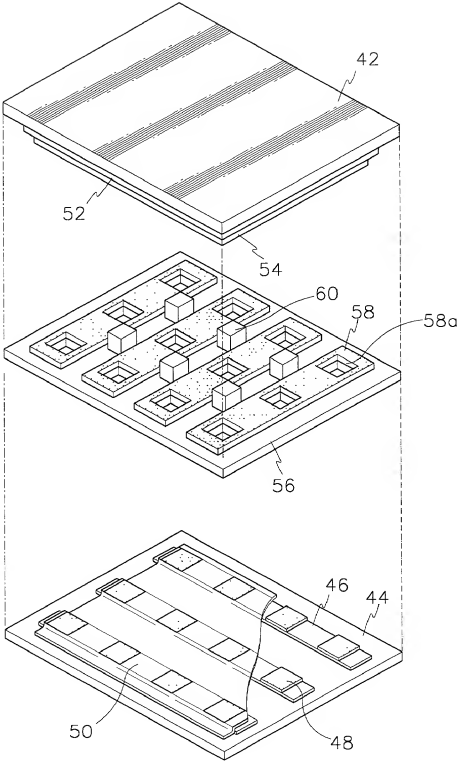


FIG.18

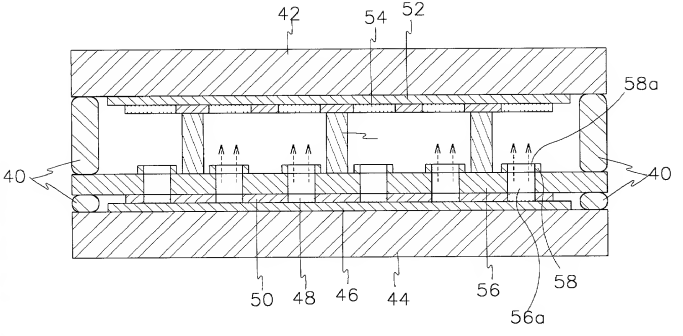


FIG.19

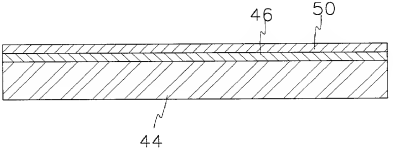


FIG.20

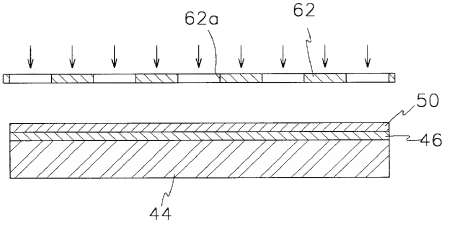


FIG.21

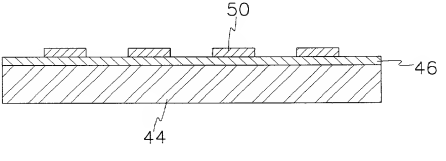


FIG.22

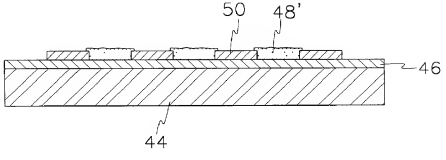
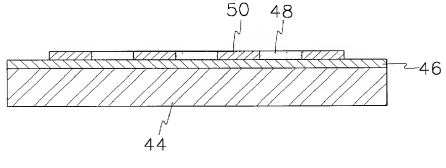


FIG.23



Rev. 4/97 **DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATIONS** PATENT

Docket No.: 40176/DBP/Y35
Attorney : D. Bruce Prout

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **"FLAT PANEL DISPLAY AND METHOD OF FABRICATING SAME"**, the specification of which is attached hereto unless the following is checked:
___ Was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

1 hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of the foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Application Number	Country	Filing Date (day/month/year)	Priority Claimed
1999-35034	**Korea**	**23/08/1999**	**Yes**
1999-44602	**Korea**	**14/10/1999**	**Yes**
2000-80	**Korea**	**03/01/2000**	**Yes**

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Application Number	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, 1 acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

Application Number	Filing Date	Patented/Pending/Abandoned

POWER OF ATTORNEY: I hereby appoint the following attorneys and agents of the law firm CHRISTIE, PARKER & HALE, LLP to prosecute this application and any international application under the Patent Cooperation Treaty based on it and to transact all business in the U.S. Patent and Trademark Office connected with either of them in accordance with instructions from the assignee of the entire interest in this application; or from the first or sole inventor named below in the event the application is not assigned; or from YOU ME PATENT & LAW FIRM in the event the power granted herein is for an application filed on behalf of a foreign attorney or agent.

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATIONS

Docket No.: 40176/DBP/Y35

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The authority under this Power of Attorney of each person named above shall automatically terminate and be revoked upon such person ceasing to be a member or associate of or of counsel to that law firm.

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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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